ABSTRACT OF THE DISCLOSURE

A transceiver circuit comprising state machine(s) having tone phase(s) and data transfer phase(s), error detection circuit(s) detecting error(s) in receive signal(s), and phase transition suppressor circuit(s); wherein, in the event that it is determined as a result of error detection that channel quality is so poor as to make it impossible to carry out normal data transfer, transition may be made from data transfer phase(s) to tone phase(s), and by thereafter preventing transition back to data transfer phase(s) and/or speed negotiation phase(s), power consumption as would be consumed by high-speed circuit(s) when in data transfer phase(s) and/or speed negotiation phase(s) may be reduced or eliminated. Furthermore, by suppressing generation of BUS_RESET(s) due to error(s) during data transfer phase(s), reduction in bus power consumption and/or improved bus stability may be achieved.